PHASE- AND DELAY-LOCKED LOOP CLOCK CONTROL IN DIGITAL SYSTEMS

Zeljko Zilic

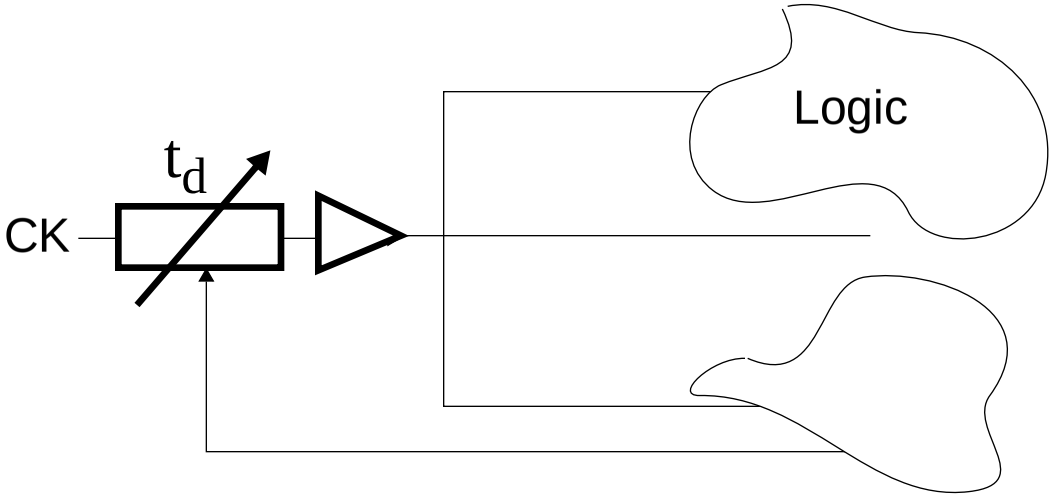
- Clock distribution problem in synchronous systems
  - Jitter and clock skew
- Use of Phase-Locked Loops (PLLs) and Delay-Locked Loops (DLLs) in digital systems
- PLL/DLL building elements for digital designers
- Dynamic clock management issues

PLLs/DLLs: Why Bother?

- No need to use PLLs in digital systems on chip ~5 years ago
- Recent increase in digital logic speed and level of integration
  - Communication applications need PLLs/DLLs
- Synchronous circuit speed: degraded by clock skew
  - Clock cycles of 10ns (100 MHz) cannot tolerate few ns of clock skew
- PLLs introduce closed-loop timing compensation, as opposed to open-loop clock skew reduction mechanisms
  - Clock tree distributions and skew tolerance schemes are open-loop schemes that can reduce, but not eliminate skew

CLOSED-LOOP SKEW COMPENSATION

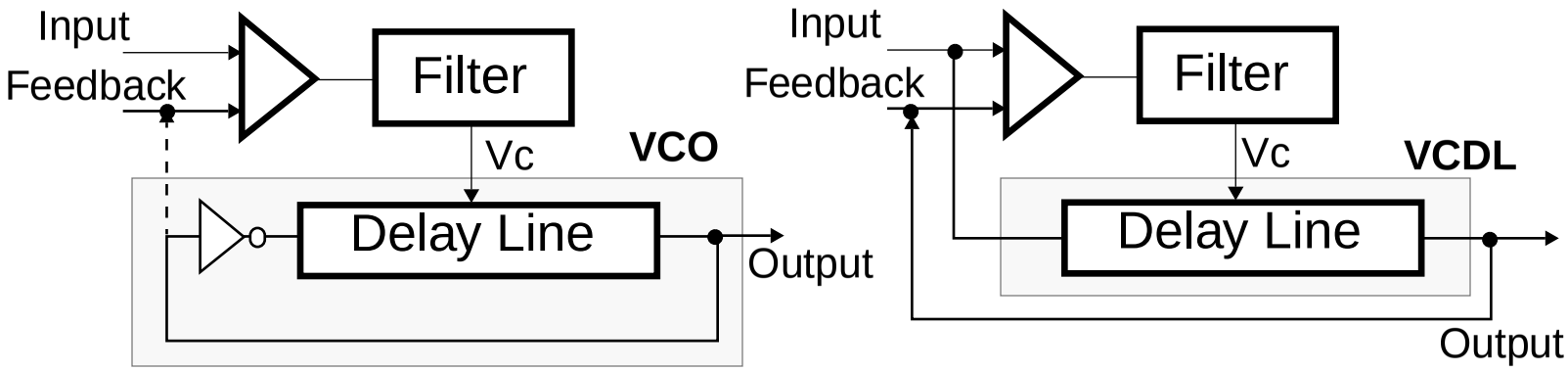
- Clock skew is measured and compensated by a control loop
  - Sources outside the loop are uncompensated
- Typical situtation: loop around the buffer



  - Inserts negative delay!

PHASE- AND DELAY-LOCKED LOOPS

- Two closed-loop skew control mechanisms
- Both circuits align input clock with selected feedback signal

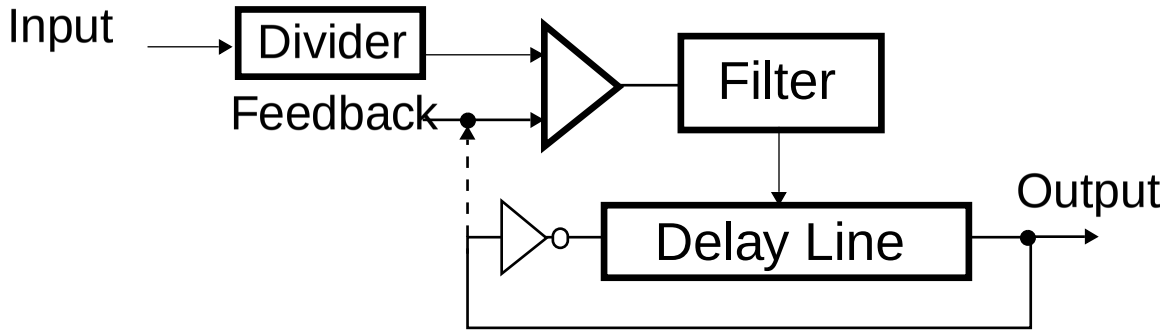


Phase-Locked Loop Delay-Locked Loop

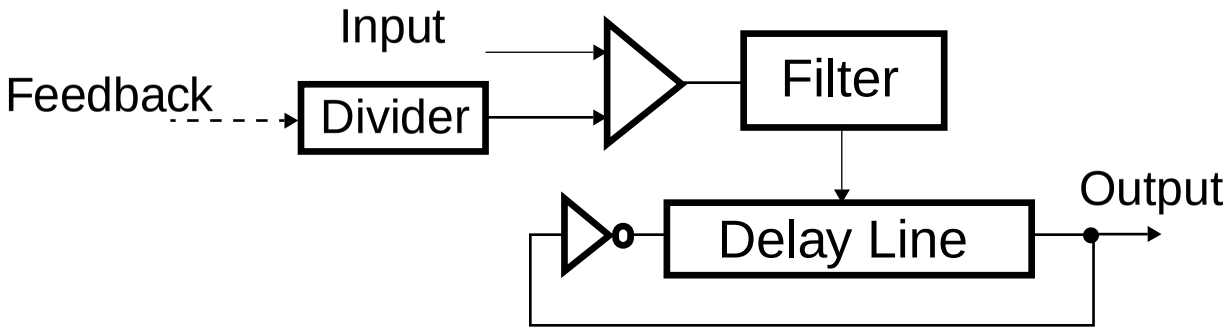
- Voltage controlled ring oscillator (VCO) vs. voltage controlled delay line (VCDL)
  - Control voltage: Vc

PLLs in Frequency Synthesis

- Dividing clock rate



- Multiplying clock rate

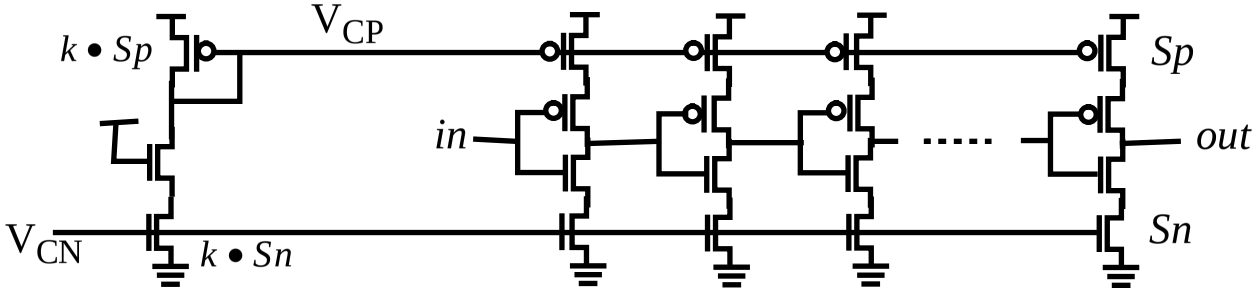


VOLTAGE CONTROLLED OSCILLATORS

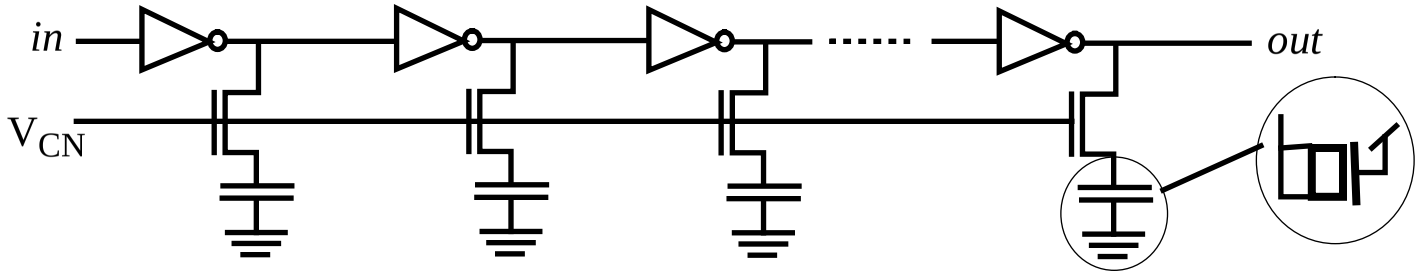
- Core of the PLLs/DLLs - oscillators that can be controlled by voltage (or current)
  - Ideally, frequency is proportional to control voltage
- Our application: square wave is usually obtained by a delay line acting as a ring oscillator
  - Ring with odd number of inverters
- Good VCOs must have the following
  - Low intrinsic jitter
  - High power supply noise rejection ratio

DELAY LINE IMPLEMENTATIONS

- Current-starved inverter delay line

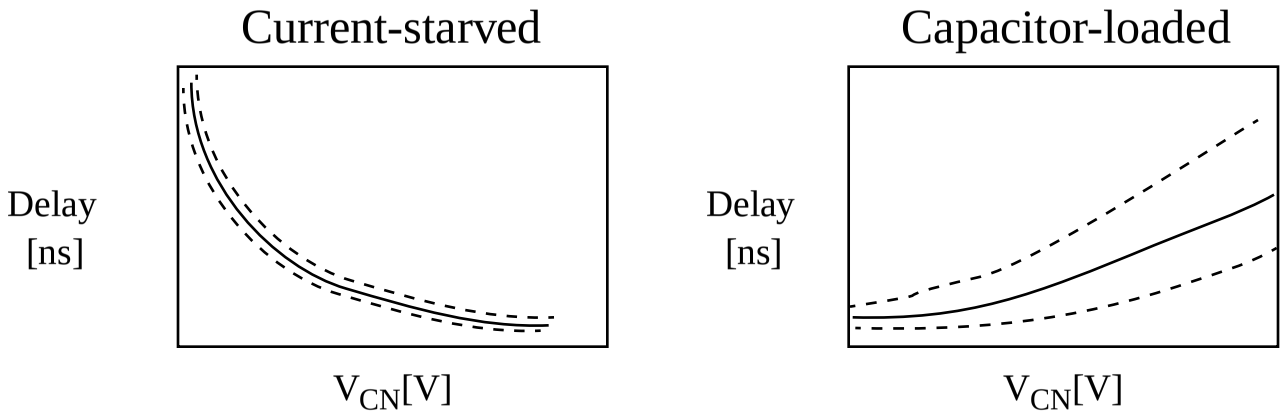


- Capacitor-Loaded inverter delay line



DELAY ADJUSTMENT RANGE

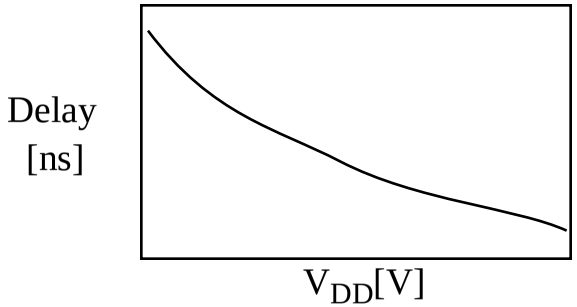
- Cannot have both large range of delays and fine-grain adjustments
- Current-starved vs. capacitor-loaded delay line



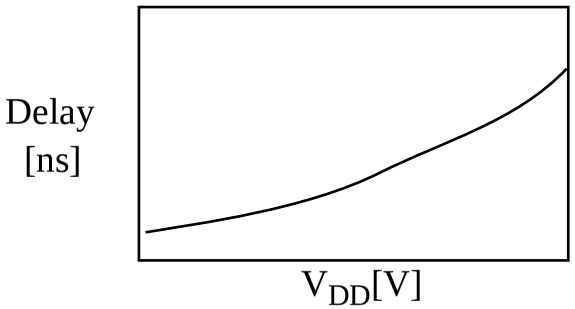
- Delay line with N delay elements has N taps. By allowing each tap to be used, the range is extended

SUPPLY NOISE REJECTION

- Noise rejection of CMOS inverters

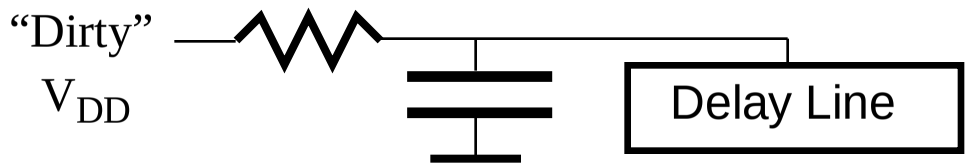


- Supply sensitivity of current-starved inverter delay line

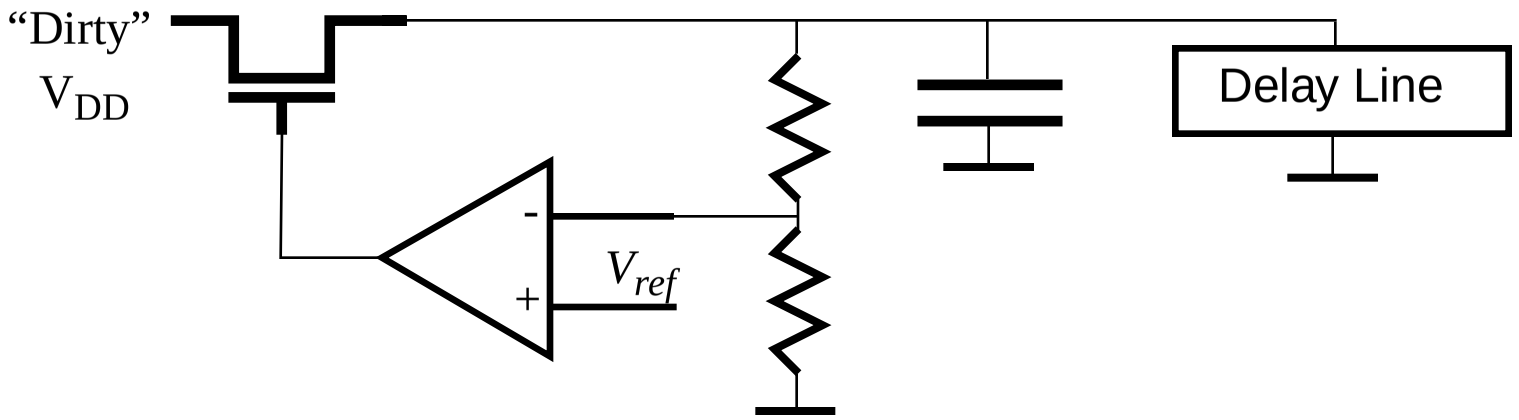


REDUCING POWER SUPPLY NOISE

- Improve the power supply
  - Passive: Low-pass filter

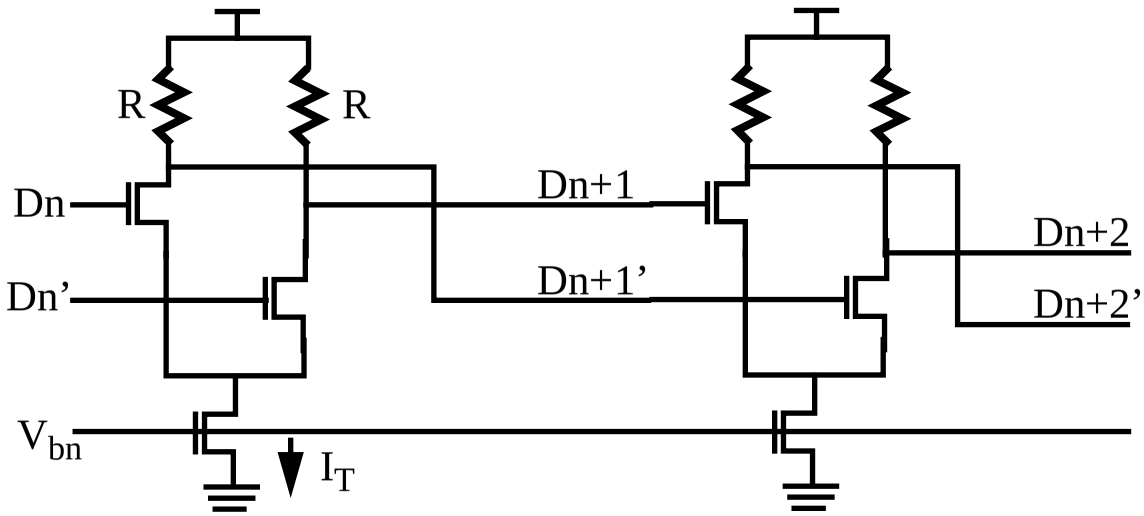


  - Active: Linear regulated power supply



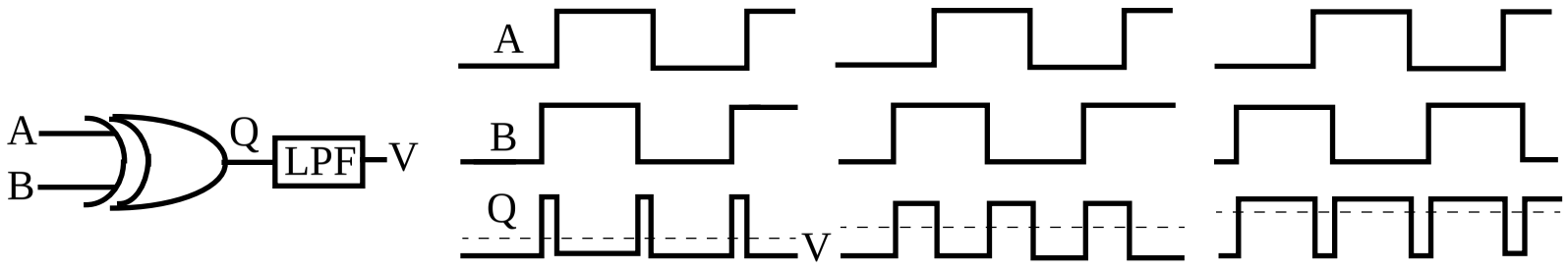
LIVING WITH POWER SUPPLY NOISE

- Use differential delay elements
- Differential inverter chain
- Or, the following circuit:

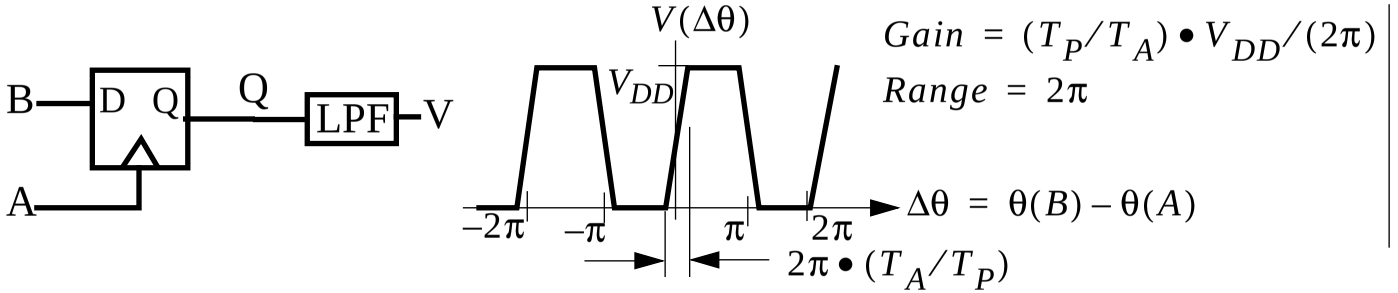


PHASE COMPARATORS

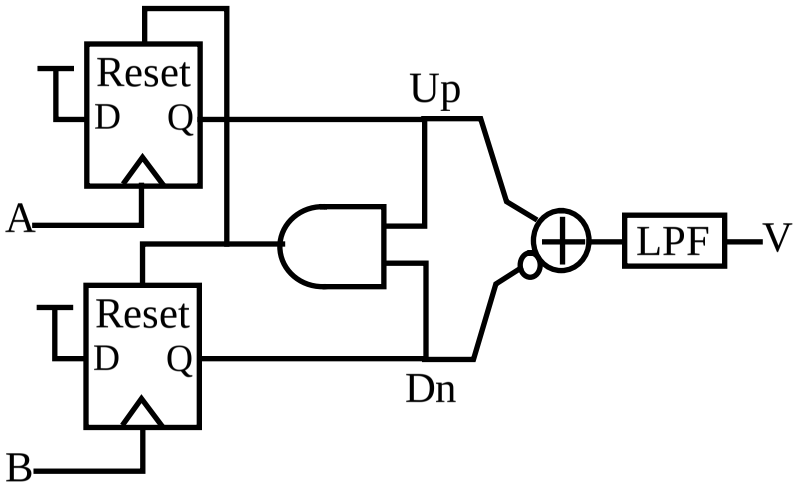
- XOR Based

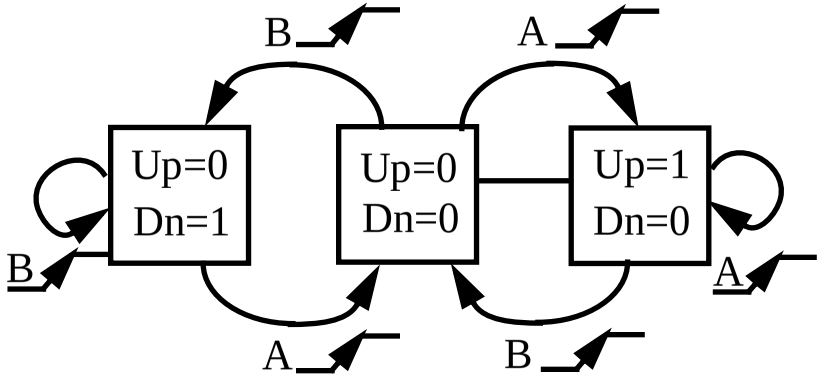


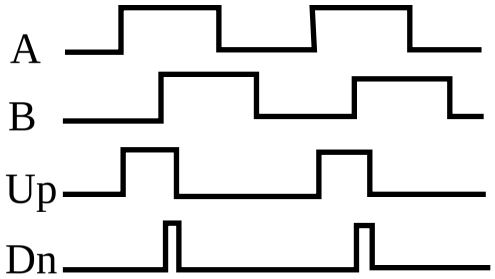
- Sequential

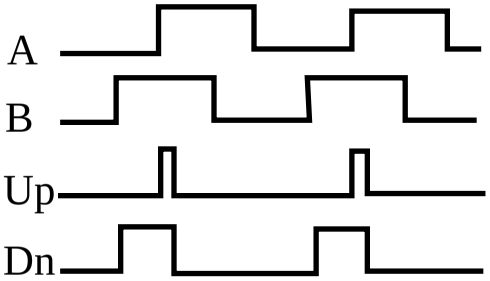


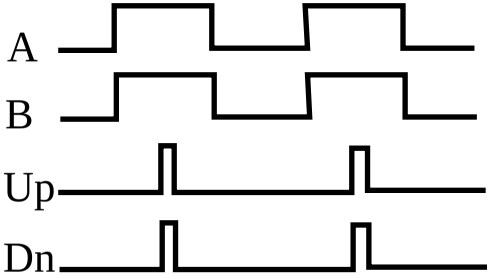
PHASE FREQUENCY DETECTOR





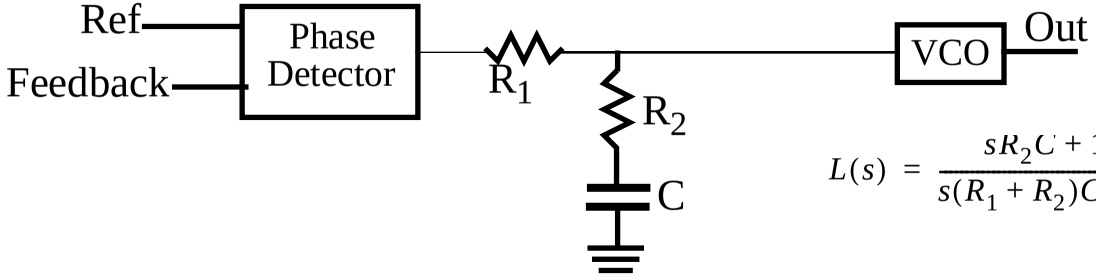






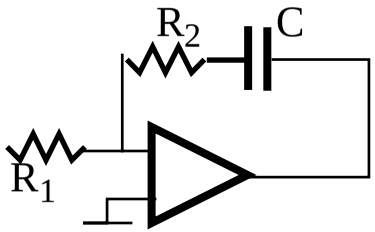
LOOP FILTERS

- Function: controlling the loop dynamics
  - Removes high-frequency (noise), stabilizes the response
- Passive filters: RC network



$$L(s) = \frac{sR_2C + 1}{s(R_1 + R_2)C + 1}$$

- Active filter:



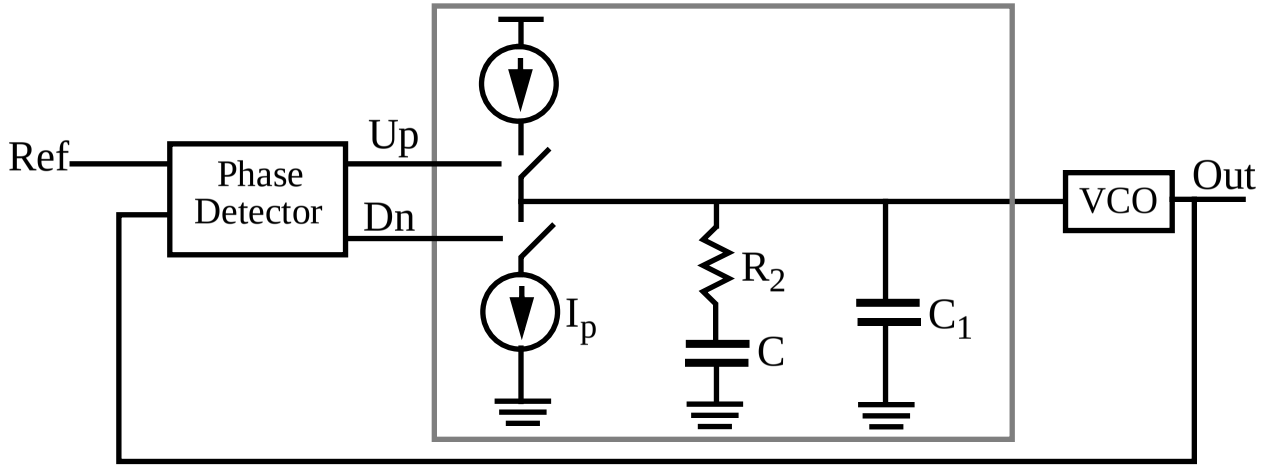
$$L(s) = \frac{(sR_2C + 1)}{sR_1C}$$

Osc. Frequency ω_1 and dumping factor

$$\omega_1 = \sqrt{\frac{K_{PD}K_{VCO}}{R\ C}}, \quad \zeta = \omega_1\frac{R_2C}{2}$$

CHARGE PUMP PLLS

- Typical Implementation



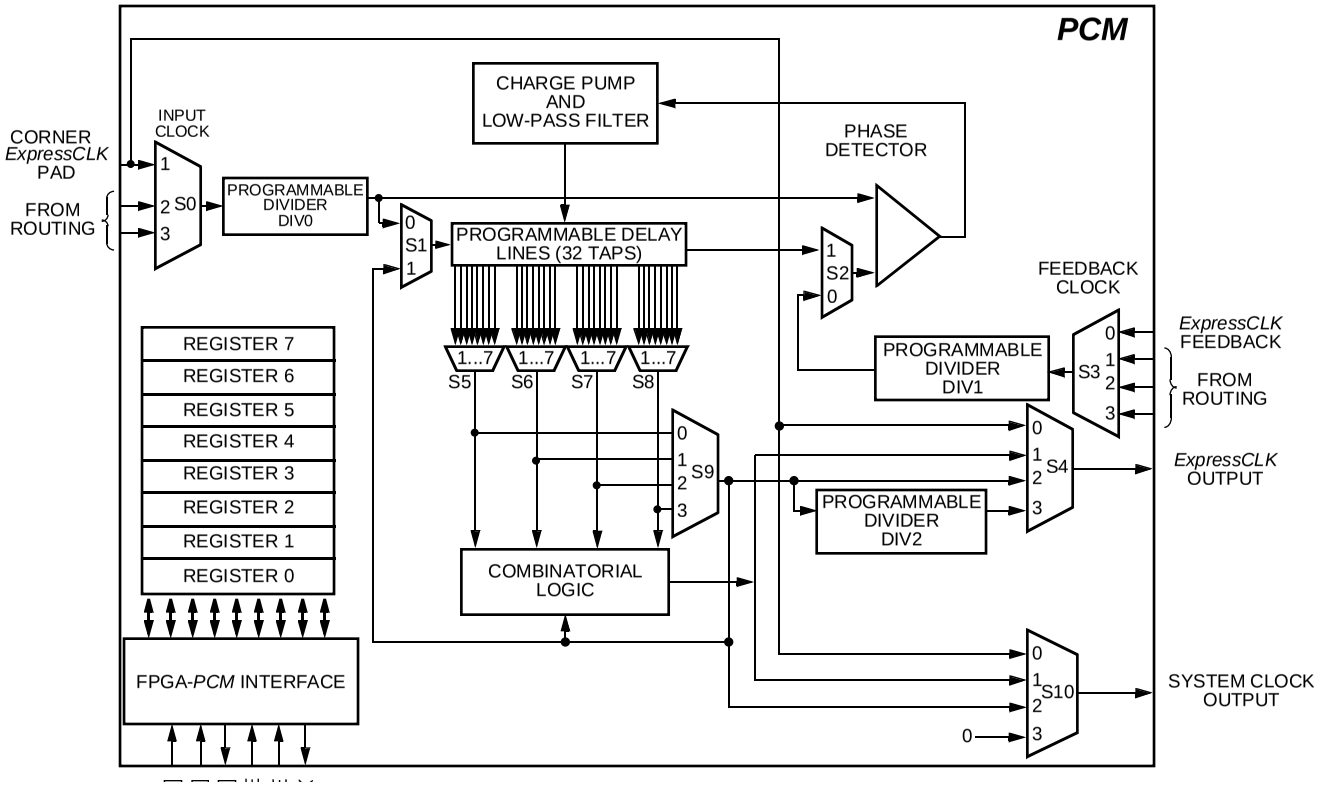
- Loop stability: comparable to active filter
  - Want: high osc. frequency ω_1. (Rule of thumb: 1/10 of reference clock.)

DLL IMPLEMENTATIONS

- DLLs stability simpler to analyze: first order systems
  - First order loop filters suffice
- However, many complications:
- *False lock* problem: DLL loop delay is not T, but one of: 0T, 2T, ... nT, ...
  - Resolving problem: (digital) circuits that disable false lock
- “Turbo” mode: allows fast acquisition by more current in charge-pump
- Bang-Bang Controller: high-gain detectors with rapid capture, but small clock phase excursions

CLOCK MANAGER EXAMPLE

- ORCA FPGA Programmable Clock Manager



CLOCK MANAGER USE

- PLL mode: close delay line ring
- PLL frequency multiplication by M: divide feedback by M
- PLL frequency multiplication by M/N: above plus N in output divider
- DLL mode: delay line fed by input
- DLL programmable delay: select tap X as output
- DLL duty cycle adjustment: select tap X as to duty cycle circuit
- DLL clock multiplication/duty cycle adjustment: select tap X and tap 16+X as inputs to clock doubler

DYNAMIC CLOCK MANAGEMENT

- Low power applications: run as fast as needed, no faster
  - Impossible with current clock managers
- Dynamic clock management problems:
  - Clock dividers work incorrectly
    - Oscillations in forbidden states
    - Transient behaviors
  - VCOs work inefficiently, need external programming
    - PLLs might not achieve locking range
    - Need external intervention to adjust VCO length
    - Transient behaviors
    - Slow response
- Solutions: Patented Dynamic Clock Divider, PLL